CLAIMS

1. An apparatus for automatically activating a clock master circuit in a stack of Fast Ethernet repeaters comprising:

a first stackable Fast Ethernet repeater including:

a first on pin having a first on pin logical state, the first on pin logical state being indicative of whether or not the first stackable Fast Ethernet repeater is configured in the stack of Fast Ethernet repeaters so that no other Fast Ethernet repeater occupying a position in the Fast Ethernet repeater stack that is before the position of the first Fast Ethernet repeater is powered on;

a weak pull up voltage source connected to the first on pin, the weak pull up voltage being derived from a switched power supply in the Fast Ethernet repeater so that when the Fast Ethernet repeater is powered on, the weak pull up voltage is present and when the Fast Ethernet repeater is powered off, the weak pull up voltage is not present; and

a clock master circuit having an enable input wherein the enable input is controlled by the first on pin logical state;

a second stackable Fast Ethernet repeater including a power state output pin, the power state output pin being configured to be connected to ground when the second Fast Ethernet repeater is powered on; and

a connector cable running from the first Fast Ethernet repeater to the second Fast Ethernet repeater, the connector cable connecting the first on pin from the first stackable Fast Ethernet Repeater to the power state output pin of the second stackable Fast Ethernet repeater.

whereby the clock master circuit in the first stackable Fast Ethernet Repeater is enabled based on whether the second stackable Fast Ethernet repeater is powered on.

2. An apparatus for automatically activating a clock master circuit in a stack of Fast Ethernet repeaters as recited in claim 1 wherein the power state output pin is configured to float when the Fast Ethernet repeater is powered on.

3. An apparatus for automatically activating a clock master circuit in a stack of Fast Ethernet repeaters as recited in claim 1 wherein the power state output pin is configured to be connected to a second stackable Fast Ethernet repeater first on pin on a second stackable Fast Ethernet repeater when the second stackable Fast Ethernet repeater is powered off so that the state of the second stackable Fast Ethernet repeater first on pin is transferred to the first on pin of the first stackable Fast Ethernet repeater when the second stackable Fast Ethernet repeater is powered off.

4. An apparatus for automatically activating a clock master circuit in a stackable Fast Ethernet repeater comprising:

a local input connector including a local first on pin having a first on pin logical state, the local first on pin logical state being indicative of whether or not the stackable Fast Ethernet repeater is configured in a stack of Fast Ethernet repeaters in a manner indicating that the Fast Ethernet repeater is not selected to activate the clock master circuit and wherein the local input connector is configured to connect the local first on pin to a remote power state output pin on a remote output connector when the local input connector is connected to the remote output connector;

a weak pull up voltage source connected to the local first on pin, the weak pull up voltage being derived from a switched power supply in the Fast Ethernet repeater so that when the Fast Ethernet repeater is powered on, the weak pull up voltage is present and when the Fast Ethernet repeater is powered off, the weak pull up voltage is not present; and

a clock master circuit having an enable input wherein the enable input is controlled by the first on pin logical state;

whereby the clock master circuit is enabled according to the state of the local first on pin and the local first on pin is pulled high by the weak pull up voltage unless the local first on pin is connected to a remote power state output pin that pulls the local first on pin low.

5. An apparatus for automatically activating a clock master circuit in a stackable Fast Ethernet repeater as recited in claim 4 further including a local output connector having a local power state output pin configured to be connected to ground when the Fast Ethernet repeater is powered on and configured to be allowed to float when the Fast Ethernet repeater is powered off.

6. An apparatus for automatically activating a clock master circuit in a stackable Fast Ethernet repeater as recited in claim 4 further including a local output connector having a local power state output pin configured to be connected to ground when the Fast Ethernet repeater is powered on and configured to be connected to the local first on pin when the Fast Ethernet repeater is powered off.

7. A method of automatically activating a clock master circuit in a stack of Fast Ethernet repeaters comprising:

selectively connecting a first on pin in a first stackable Fast Ethernet repeater to a weak pull up voltage source when the first stackable Fast Ethernet repeater is powered on;

connecting the first on pin in the first stackable Fast Ethernet repeater to a power state output pin in a second stackable Fast Ethernet repeater wherein the power state output pin is configured to be connected to ground when the second Fast Ethernet repeater is powered on; and

enabling a clock master circuit having an enable input based on the voltage on the first on pin.

8. A method of automatically activating a clock master circuit in a stack of Fast Ethernet repeaters as recited in claim 7 further including connecting the power state output pin to ground when the second Fast Ethernet repeater is powered on and allowing the power state output pin to float when the second Fast Ethernet repeater is powered off.

9. A method of automatically activating a clock master circuit in a stack of Fast Ethernet repeaters as recited in claim 7 further including connecting the power state output pin to the a second stackable Fast Ethernet repeater first on pin on the second stackable Fast Ethernet repeater when the second stackable Fast Ethernet repeater is powered off so that the state of the second stackable Fast Ethernet repeater first on pin is transferred to the first on pin of the first stackable Fast Ethernet repeater when the second stackable Fast Ethernet repeater is powered off.